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High field transport of high performance black phosphorus transistors

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Black phosphorus is a layered material stacked together by weak van der Waals force with a direct bandgap and highly anisotropic electrical characteristics. Most of the previous reports focus on the low-field mobility of transistors based on SiO_2 back gate dielectrics. Recently, black phosphorus transistors encapsulated with hexagonal boron nitride have been demonstrated with greatly improved mobility at low temperatures. However, this approach requires multiple dry transfer methods using both black phosphorus and boron nitride flakes, which are only available in small crystal sizes. Here, we demonstrated high performance black phosphorus transistors using atomic layer deposited high-κ HfO_2 as a back gate dielectric. The maximum drain current density reaches 480 μA/μm at 300 K and a record high drain current 906 μA/μm at 20 K in a short channel 100 nm device based on HfO_2, exhibiting excellent current-carrying capability and high field strength. Moreover, a side-by-side comparison on important figures-of-merit is carried out systematically for transistors based on HfO_2 with those based on conventional SiO_2, showing more than 50% performance improvement in mobility and over 8 times reduction in interface trap density. *Published by AIP Publishing.*
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Black phosphorus (BP) is a layered material stacked together by weak van der Waals force, and recent experiments show that few layer BP can be obtained by mechanical exfoliation for next generation electronic and optical applications.[1–4] It was found that the bandgap strongly depends on the number of layers changing from ~0.3 eV in the bulk to ~2 eV in the monolayer and remains to be the direct bandgap.[5–7] This wide span of bandgap is appealing because it fills the energy spectrum gap between zero-bandgap graphene and relatively large-bandgap transition metal dichalcogenides (TMDs), covering from the visible to infrared range suitable for optoelectronics.[8–12] Moreover, BP is very attractive for electronic applications such as in field effect transistors (FETs) because of its high mobility ranging from 10^2 to 10^4 cm^2/Vs, which is larger than that of most of the TMD materials, making it a strong candidate for future thin film transistors and flexible analog and logic devices.[13–17] Recently, black phosphorus transistors encapsulated with hexagonal boron nitride have been demonstrated with greatly improved mobility at low temperatures. However, this approach require multiple dry transfer methods using both black phosphorus and boron nitride flakes, which are only available in small crystals.[18–20] It has been shown experimentally that the presence of high-κ dielectrics in TMD devices can improve the device performance, and similar results have also been reported in BP FETs.[21–27] Despite the tremendous research efforts on BP electronic devices in the past few years, the high field transport and current carrying capability of BP devices are still largely missing. In this letter, we perform a comprehensive study on the most important figures-of-merit such as on-state current, mobility, and interface trap density of BP FETs based on high-κ HfO_2 dielectrics in comparison to SiO_2 and push their high field transport much further beyond the current status.

BP FETs on heavily p-doped silicon (p^{++} Si) wafers covered with 90 nm SiO_2 and 25 nm HfO_2 are shown in the schematic views of Fig. 1(a). 25 nm HfO_2 was grown by atomic layer deposition (ALD) with a dielectric constant of around 13. Few layer BP flakes were mechanically exfoliated and then transferred onto the substrate. The BP flakes used

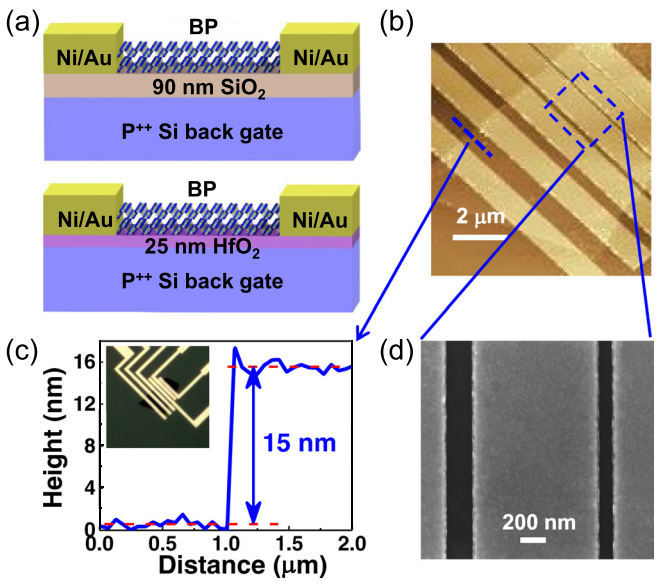

FIG. 1. (a) Schematic view of BP FETs. The back gate dielectrics are 90 nm SiO_2 (Top) and 25 nm HfO_2 (Bottom) for two types of device configuration, respectively. (b) The AFM image of a typical transistor array for exfoliated back gate BP devices. Scale bar: 2 μm. (c) The measured height along the blue dashed line in panel (b) is about 15 nm, and the inset shows the corresponding optical image of the device array. (d) SEM image of the 100 nm and 200 nm channel device. Scale bar: 200 nm.

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for both types of device fabrication were carefully chosen to be the same thickness of around 15 nm, which are verified by atomic force microscopy (AFM) as shown in Figs. 1(b) and 1(c). E-beam lithography was used to pattern the source/drain electrodes, and 15 nm Ni/40 nm Au was deposited by e-beam evaporation to form the source/drain contact, as shown in the inset of Fig. 1(c). Fig. 1(d) shows a scanning electron microscopy image of the device with a channel length down to 100 nm.

The transfer characteristics of BP FETs on SiO_2 and HfO_2 at various temperatures are shown in Figs. 2(a) and 2(b), respectively. The channel length is 500 nm with $V_{ds} = -0.05$ V. Both BP FETs show nearly a similar on/off ratio of $\sim 10^2$ at 300 K and $\sim 10^3$ at 70 K, which further confirms the identical thickness of the two BP flakes. The improvement in the on/off ratio at low temperature is mainly due to the reduction in carrier density in the off-state. In comparison to the BP FET on the SiO_2 device, the device on HfO_2 shows a steeper subthreshold slope (SS). This is a clear indication that high-κ dielectrics have advantages of smaller equivalent oxide thickness (EOT), and as a result, they can achieve much tighter electrostatic control by the back gate. Besides, the gate voltage of the minimum current $V_{bg,min}$ for BP on SiO_2 shifted greatly from 35 V to 20 V as the temperature decreases from 300 K to 70 K, while it changes little for BP on HfO_2. The huge difference in this shift of the minimum current point can be better seen from the comparison in Fig. 2(c), where the y-axis range of the two types of oxide scales with the gate capacitance to make a fair comparison. The temperature dependent minimum current point shift is mainly due to the frozen trap charges at the oxide/BP interface at low temperatures. It is clear that trap charges located at the SiO_2/BP interface are much larger than those of the HfO_2/BP interface, which start to freeze out below 220 K. We use the minimum current point at 70 K as a reference point, and the trap charge density at 300 K is estimated to be around $3.3 \times 10^{12}/cm^2$ for SiO_2/BP using the equation $n_{trap} = C_{ox}\Delta V_{bg,min}/q$ and approximately $3.9 \times 10^{11}/cm^2$ for HfO_2/BP, which shows a reduction in trap density for more than eight times, as shown in the inset of Fig. 2(c).

Moreover, field-effect mobility can be extracted from the transfer characteristics in the linear region using the equation $\mu_{FE} = g_m L_{ch}/WC_{ox}V_{ds}$, where g_m is the peak transconductance extracted from the I_{ds}-V_{bg} curve, L_{ch} and W are the channel length and width, respectively, C_{ox} is the back gate capacitance, and V_{ds} is the drain-to-source voltage. To eliminate the parasitic effects from contact resistance, the effective V_{gs}, V_{ds}, and intrinsic transconductance are given by $V'_{gs} = V_{gs} - I_{ds}R_C$, $V'_{ds} = V_{ds} - 2I_{ds}R_C$, and $g'_m \approx g_m/(1 - R_C g_m)$,[28] respectively, where R_C is the contact resistance extracted by the transfer length method. Fig. 2(d) shows the intrinsic mobility versus temperature of a 500 nm device. A hole mobility of 200 cm^2/Vs has been achieved in BP FETs on HfO_2 at 300 K, a 100% enhancement when compared with that on SiO_2. The mobility is always >1.5 times higher on HfO_2 than that on SiO_2 in the entire temperature range, which can be attributed to the effective screening of trap charge scattering and reduction in trap density due to the presence of the HfO_2 dielectric.[23,29,30] The output characteristics of the BP FETs with a channel length of 500 nm on SiO_2 and HfO_2 at room temperature are shown in Fig. 3(a). The on-state current (I_{on}) for BP on SiO_2 is 244 μA/μm, while I_{on} for BP on HfO_2 is 348 μA/μm, a 43% enhancement. Note here that the back gate voltage applied on the device scales with the back gate capacitance ratio ($C_{HfO2}/C_{SiO2} = 12$), so as to make sure that the carrier density in the channel is almost the same for a fair comparison where the main contributing factor is mobility at the low field. Fig. 3(b) shows the output characteristics for both devices at 70 K, where the I_{on} increases to 300 μA/μm for BP on SiO_2 and to 450 μA/μm for BP on HfO_2, which shows a similar improvement of more than 50% for the HfO_2 device. Although the drain current starts to show non-linear behavior due to the Schottky barrier effect at low temperatures, the on-state current still increases for more than 25% compared to room temperature, which can be attributed to greatly increased mobility.

In order to evaluate the current carrying capacity, shorter channel devices should be characterized where the electric field in the channel can be enhanced. The temperature dependent I_{on} for two 100 nm devices is summarized in Fig. 4(a), showing a monotonic increase in current with decreasing temperature for both types of devices. This improvement can be attributed to the increasing mobility due to the reduced scatterings from both interface traps and surface phonons at low

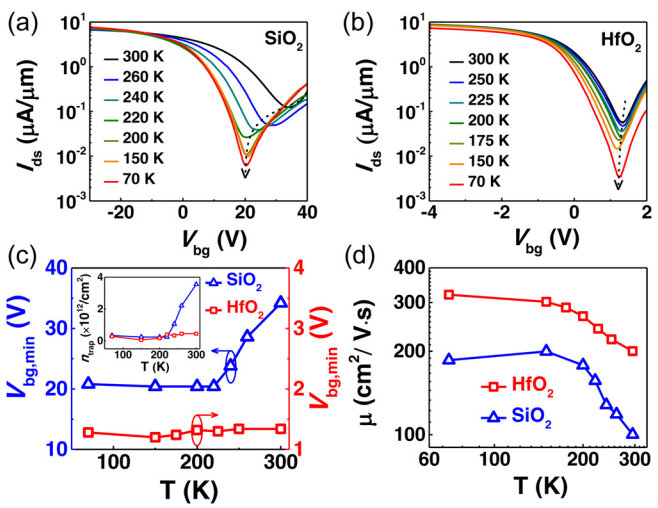

FIG. 2. Transfer characteristics of a 500 nm device for BP on SiO_2 (a) and HfO_2 (b) at different temperatures; $V_{ds} = -0.05$ V. (c) The gate voltage point of the minimum current $V_{bg,min}$ versus temperature. The inset shows trap charge density for both types of transistors. (d) Intrinsic field-effect mobility versus temperature for both types of transistors.

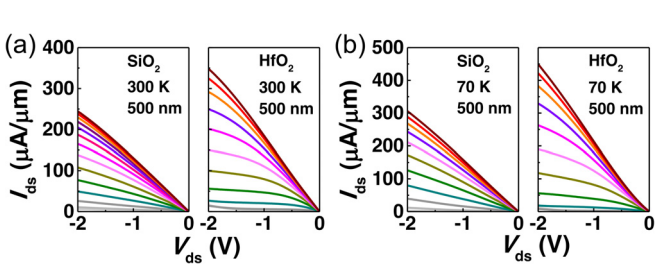

FIG. 3. Output characteristics of a 500 nm device for BP on SiO_2 and HfO_2 at 300 K (a) and 70 K (b). V_{bg} varies from 30 V to −30 V with a step of −5 V for BP on SiO_2, and V_{bg} varies from 1 V to −4 V with a step of −0.5 V for BP on HfO_2.

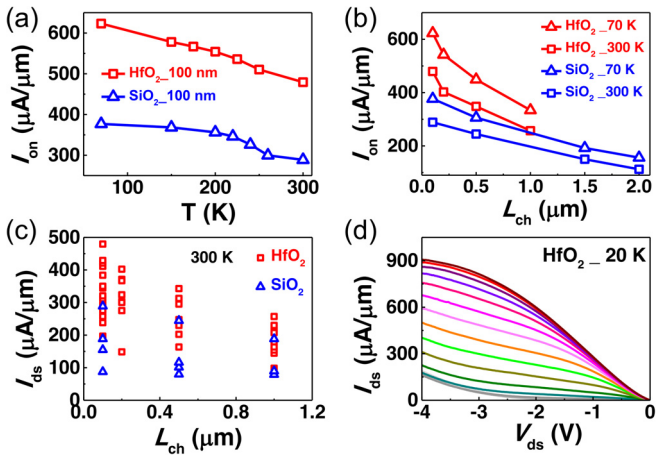

FIG. 4. (a) On-state current (I_{on}) versus temperature with $L_{ch} = 100$ nm at $V_{ds} = -2$ V. (b) On-state current versus channel lengths at 300 K and 70 K. (c) Statistics data of the on-state current as a function of channel length at 300 K. (d) Output characteristics of the 100 nm device on HfO_2 at 20 K, and V_{bg} varies from 1 V to −6 V with a step of −0.5 V.

temperatures. The on-state currents of 480 μA/μm of the 100 nm HfO_2 device at 300 K and 623 μA/μm at 70 K can be achieved with $V_{ds} = -2$ V. Fig. 4(b) shows the systematic study of I_{on} with different channel lengths at 300 K and 70 K, where the on-state current increases as the channel length scales down, and it is always higher for the HfO_2 device than that for the SiO_2 device. This behavior shows great potential for performance improvement in BP devices with further interface optimization and channel length scaling down. Fig. 4(c) shows the statistics data of I_{on} as a function of channel length for both types of devices at 300 K. The overall performance of HfO_2 devices is better than that of the SiO_2 devices. To further push the current carrying capability, we increase the drain voltage to −4 V at a lower temperature of 20 K. An output current of 906 μA/μm was obtained as shown in Fig. 4(d), the largest drive current achieved in BP FETs to date.[31–33]

In summary, we have fabricated BP FETs using atomic layer deposited HfO_2 as a gate dielectric, and key figures-of-merit such as mobility and interface qualities have been studied systematically for a wide temperature range, exhibiting greatly improved device performance in comparison to the BP FETs on conventional SiO_2. A record high drain current of 906 μA/μm at 20 K has been achieved for a 100 nm device on HfO_2, demonstrating excellent current-carrying capability of BP as a channel material. These results provide insights into important device characteristics of BP based transistors and show great potential for future high performance electronic devices based on two dimensional materials.

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[1]L. Li, Y. Yu, G. J. Ye, Q. Ge, X. Ou, H. Wu, D. Feng, X. H. Chen, and Y. Zhang, Nat. Nanotechnol. **9**, 372 (2014).
[2]F. Xia, H. Wang, and Y. Jia, Nat. Commun. **5**, 4458 (2014).
[3]H. Liu, A. T. Neal, Z. Zhu, Z. Luo, X. Xu, D. Tománek, and P. D. Ye, ACS Nano **8**, 4033 (2014).
[4]Y. Liu, T. Low, and P. Paul Ruden, Phys. Rev. B **93**, 165402 (2016).
[5]J. Qiao, X. Kong, Z.-X. Hu, F. Yang, and W. Ji, Nat. Commun. **5**, 4475 (2014).
[6]V. Tran, R. Soklaski, Y. Liang, and L. Yang, Phys. Rev. B **89**, 235319 (2014).
[7]Y. Akahama, S. Endo, and S.-I. Narita, J. Phys. Soc. Jpn. **52**, 2148 (1983).
[8]H. O. H. Churchill and P. Jarillo-Herrero, Nat. Nanotechnol. **9**, 330 (2014).
[9]F. Xia, H. Wang, D. Xiao, M. Dubey, and A. Ramasubramaniam, Nat. Photonics **8**, 899 (2014).
[10]M. Buscema, D. J. Groenendijk, S. I. Blanter, G. A. Steele, H. S. J. van der Zant, and A. Castellanos-Gomez, Nano Lett. **14**, 3347 (2014).
[11]N. Youngblood, C. Chen, S. J. Koester, and M. Li, Nat. Photonics **9**, 247 (2015).
[12]M. Huang, M. Wang, C. Chen, Z. Ma, X. Li, J. Han, and Y. Wu, Adv. Mater. **28**, 3481 (2016).
[13]S. Das, W. Zhang, L. Raju Thoutam, Z. Xiao, A. Hoffmann, M. Demarteau, and A. Roelofs, IEEE Electron Device Lett. **36**, 621 (2015).
[14]H. Wang, X. Wang, F. Xia, L. Wang, H. Jiang, Q. Xia, M. L. Chin, M. Dubey, and S-j. Han, Nano Lett. **14**, 6424 (2014).
[15]J. S. Kim, P. J. Jeon, J. Lee, K. Choi, H. S. Lee, Y. Cho, Y. T. Lee, D. K. Hwang, and S. Im, Nano Lett. **15**, 5778 (2015).
[16]A. D. Franklin, Science **349**, aab2750 (2015).
[17]W. Zhu, S. Park, M. N. Yogeesh, K. M. McNicholas, S. R. Bank, and D. Akinwande, Nano Lett. **16**, 2301 (2016).
[18]X. Chen, Y. Wu, Z. Wu, Y. Han, S. Xu, L. Wang, W. Ye, T. Han, Y. He, Y. Cai, and N. Wang, Nat. Commun. **6**, 7315 (2015).
[19]L. Li, F. Yang, G. J. Ye, Z. Zhang, Z. Zhu, W. Lou, X. Zhou, L. Li, K. Watanabe, T. Taniguchi, K. Chang, Y. Wang, X. H. Chen, and Y. Zhang, Nat. Nanotechnol. **11**, 593 (2016).
[20]G. Long, D. Maryenko, J. Shen, S. Xu, J. Hou, Z. Wu, W. K. Wong, T. Han, J. Lin, Y. Cai, R. Lortz, and N. Wang, Nano Lett. **16**, 7768 (2016).
[21]K. L. Ganapathi, S. Bhattacharjee, S. Mohan, and N. Bhat, IEEE Electron Device Lett. **37**, 797 (2016).
[22]Y. Cui, R. Xin, Z. Yu, Y. Pan, Z.-Y. Ong, X. Wei, J. Wang, H. Nan, Z. Ni, Y. Wu, T. Chen, Y. Shi, B. Wang, G. Zhang, Y.-W. Zhang, and X. Wang, Adv. Mater. **27**, 5230 (2015).
[23]Z. Yu, Z.-Y. Ong, Y. Pan, Y. Cui, R. Xin, Y. Shi, B. Wang, Y. Wu, T. Chen, Y.-W. Zhang, G. Zhang, and X. Wang, Adv. Mater. **28**, 547 (2016).
[24]N. Haratipour, M. C. Robbins, and S. J. Koester, IEEE Electron Device Lett. **36**, 411 (2015).
[25]Z.-P. Ling, J.-T. Zhu, X. Liu, and K.-W. Ang, Sci. Rep. **6**, 26609 (2016).
[26]N. Haratipour and S. J. Koester, IEEE Electron Device Lett. **37**, 103 (2016).
[27]N. Haratipour, S. Namgung, S.-H. Oh, and S. J. Koester, ACS Nano **10**, 3791 (2016).
[28]S. Y. Chou and D. Antoniadis, IEEE Electron Device Lett. **34**, 448 (1987).
[29]B. Radisavljevic and A. Kis, Nat. Mater. **12**, 815 (2013).
[30]Z.-Y. Ong and M. V. Fischetti, Phys. Rev. B **86**, 121409 (2012).
[31]Y. Du, L. Yang, H. Zhou, and P. D. Ye, IEEE Electron Device Lett. **37**, 429 (2016).
[32]L. Li, M. Engel, D. B. Farmer, S-J. Han, and H. S. Philip Wong, ACS Nano **10**, 4672 (2016).
[33]L. M. Yang, G. Qiu, M. W. Si, A. R. Charnas, C. A. Milligan, D. Y. Zemlyanov, H. Zhou, Y. C. Du, Y. M. Lin, W. Tsai, Q. Paduano, M. Snure, and P. D. Ye, IEEE Int. Electron Devices Meet. **2016**, 5.5.1.